Second Workshop on Pioneering Processor Paradigms (WP^3)

(proposed to be held in conjunction with HPCA-2018, Feb. 2018)

Organizers:

- John-David Wellman (IBM Research)

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- Robert Montoye (IBM Research)

    - montoye@us.ibm.com

- Ramon Bertran (IBM Research) – also serves at website and publicity chair.

    - rbertra@us.ibm.com

- Pradip Bose (IBM Research)

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Motivation and Scope:

Innovations in instruction set architecture (ISA), processor microarchitecture and supportive advances in circuit design, compilers, semiconductor technology, pre-silicon specification, modeling and validation have all been essential elements of the computer systems revolution that has transformed human society so dramatically over the last six decades or more. In the late CMOS era, with power and reliability walls already causing major paradigm shifts, the need for new innovations in cross-layer, hardware-software design and modeling are being called for to help keep the IT industry moving and growing at historical rates. In trying to forge a path of innovation, it is sometimes worth examining the past to look for major paradigm shifts in (micro)-architecture, circuits, modeling and software that helped us keep going in the face of past technology-driven disruption points. With this in mind, we started up a new workshop series on *pioneering processor paradigms (P^3),* in conjunction with HPCA 2017. The first offering was a resounding success – so with the support of the HPCA Workshop/Tutorial chairs, we would like to continue this for a few years as a regular workshop offering. (The Final Program of WP3-2017 is attached herewith for the reviewers' information).

With the help of true pioneers as well as budding new researchers, we will take a retrospective look at how past technological hurdles were circumvented through major innovations. The goal would be to learn from the past in devising new solution strategies for the future. We expect the workshop offering to be comprised of key invited talks from true pioneers as well as reviewed selections from new generation researchers and teachers who are eager to take a retrospective look in surveying past pioneering work that can teach us a lesson about solution strategies of the future. The invited pioneers and selected speakers from the younger researcher pool (spanning

the workshops offered in 2016 amd 2017) will be featured as contributing authors of the ACM SIGMICRO Oral History Project. Also, a special issue of ACM Computing Surveys or IEEE Computer, or IBM Journal of Research and Development will be organized every other year to capture the best work featured at these workshops.

Draft Call for Contributions:

The workshop on pioneering processor paradigms invites survey (or tutorial)-like submissions for review. The ideal paper would highlight a single pioneering paper (or set of papers) constituting a major processing, design, modeling or software paradigm shift in the past. In addition to explaining the context and basic concepts articulated in such work, the author(s) should draw relevant conclusions about how this pioneering work might or should influence computing paradigms of the future.

Example topic areas include (but are not limited to):

- Processing and cache taxonomy papers.

- RISC architectures and CISC-to-RISC dynamic translation support.

- Processor pipelining, super scalar processing and branch prediction innovations.

- Register renaming, out-of-order execution and precise interruption.

- Cycle-accurate processor performance modeling.

- Innovations in floating point arithmetic units and vector/SIMD acceleration.

- VLIW architectures.

- Multi-threading, multiscalar and speculative multi-threading.

- Homogeneous and heterogeneous multi-core processors; accelerator-enabled efficiency boost.

- Power, temperature, and reliability-aware computing – with associated modeling innovations.

- Compiler innovations in support of novel microarchitectural paradigms.

- Circuit design innovations in support of (micro)-architectural paradigm shifts.

Note: Ph.D dissertation research topic proposals from (junior graduate students) that contain a survey of a key paper or two to build up the motivational justification of the proposal are quite welcome, for example.

Brief bio-sketches of the organizers:

John-David Wellman is a research staff member at IBM T. J. Watson Research Center. He has over 25 years' of pre-silicon performance modeling experience at IBM. At present he is a key member of the future z Systems (mainframe) processor microarchitecture concept definition team. He holds a Ph.D from University of Michigan, Ann Arbor.

Robert Montoye is a research staff member at IBM T. J. Watson Research Center. He made pioneering contributions to the industry-first RS/6000 (POWER-1) processor and system –

specifically in terms of its floating point engine. He has over 30 years of experience at IBM. He holds a Ph.D from University of Illinois at Urbana-Champaign.

Ramon Bertran is a research staff member at IBM T. J. Watson Research Center. He represents the "budding new researchers" category that we referred to in the proposal abstract. He has just over 5 years' experience at IBM after his Ph.D degree (obtained from Barcelona Supercomputing Center). He has made pioneering new contributions in the area of automated stress microbenchmark generation – and this methodology is now an integral part of pre- and post-silicon test/validation of power, performance and noise-resilience corners of IBM POWER and mainframe processors.

Pradip Bose is the manager of *Efficient and Resilient Systems* at IBM T. J. Watson Research Center. He has over thirty-four years of experience at IBM, and was a member of the pioneering RISC super scalar project at IBM (a pre-cursor to the first RS/6000 system product). He holds a Ph.D from University of Illinois at Urbana-Champaign. He is a Fellow of the IEEE and an IBM Master Inventor.

This workshop proposal, if accepted, will be organized as an event that is co-endorsed by the IBM Academy of Technology (of which Pradip Bose is a member). This co-endorsement will help the organizers obtain approval for a special issue of IBM Journal of Research and Development to cover selected contributions from WP3-2017 and WP3-2018. In 2018, there could be special focus on pioneering processor paradigms that are emerging from recent research investments in the area of low power, resilient embedded processor and acceleration technologies (esp. those within the domain of cognitive IOT). Some of this work is sponsored, in part, by Defense Advanced Research Projects Agency (DARPA), Microsystems Technology Office (MTO) – under ongoing programs like PERFECT, CRAFT, HIVE, etc.

The FINAL PROGRAM from last year's program (2017) is attached next for the reviewers' information.

Workshop on Pioneering Processor Paradigms (WP3)

(Held in Conjunction with HPCA-2017; Saturday February 4th 2017, Austin, TX)

FINAL PROGRAM (morning): Location: Hilton Austin, Room: 415B

7:30 AM – 8:30 AM *(room: 616AB)*: Breakfast (provided by the conference)

8:30 AM – 8:40 AM: Welcome and Introduction

- Pradip Bose; on behalf of the workshop co-organizers:
  (Ramon Bertran, Pradip Bose, Robert Montoye, John-David Wellman)

8:40 AM – 9:40 AM: **Keynote – I: Prof. Yale N. Patt,**

Ernest Cockrell, Jr. Centennial Chair in Engineering
University of Texas at Austin
Talk Title: Processor Paradigms: Evolution or Disruption

9:40 AM – 10:00 AM: Stacked Memory Architectures

- Towards a memory-centric, stacked architecture for extreme-scale, data intensive computing: *John Leidel, Xi Wang and Yong Chen,* Texas-Tech University.

10:00 AM – 10:15 AM *(room: 616AB)*: Coffee/Tea Break

10:15 AM – 10:40 AM: Reconfigurable and Power-Efficient Architectures

- Two-level controlled parallel reconfigurable architectures: *Takanobu Baba, Kanemitsu Ootsu,* Utsonomiya University

- A survey of low-power NoC design techniques: *Emmanuel Ofori-Attah and Michael Opoku Agyeman,* University of Northhampton (5 minute summary: remote presentation, via skype or just telephone tie-in).

10:40 AM – 11:20 AM: Statistical Methods in Computing

- Time-randomized processors for secure and reliable high-performance computing: *David Trilla, Carles Hernandez, Jaume Abella, Francisco Javier Cazorla,* UPC and Barcelona Supercomputing Center, Barcelona

- End-to-end stochastic computing: *Carly Schulz, Mikko Lipasti,* University of Wisconsin – Madison

11:20 AM – 12:00 Noon: Retrospective Survey-I

- Efficient floating point unit design - a historical perspective: *Robert Montoye,* IBM T. J. Watson Research Center

- 12:00 Noon – 1:15 PM: LUNCH (self)

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FINAL PROGRAM (afternoon)

Location: Hilton Austin, Room: 415B

1:15 PM – 2:15 PM: Keynote-II: **Prof. Jacob A. Abraham**

> *Cockrell Family Regents Chair in Engineering*
>
> *University of Texas at Austin*
>
> Talk Title: Pioneering Paradigms in Systems Resilience

2:15 PM – 3:15 PM: Panel Session:

- **Notable Pioneering (Research) Paradigms** (that should have made it into real design, but didn't yet, or did make it in the end after lots of tweaks)

- **Panelists:** Prof. Yale Patt, Prof. Jacob Abraham, Prof. Mikko Lipasti

- **Moderator:** one of the workshop organizers

3:15 PM – 3:30 PM *(room: 616AB)*: Coffee/Tea Break

3:30 PM – 4:15 PM: Retrospective Survey-II

- Cycle-accurate simulation advances in support of efficient & resilient design: *John-David Wellman (with Ramon Bertran and Pradip Bose),* IBM T. J. Watson Research Center

4:15 PM – 5 PM: Recap/discussion; action items

- Discussion driven by J-D Wellman, Ramon Bertran and Robert Montoye

  o Can/should we try a special issue of IEEE Computer (or ACM Communications) to cover selected articles that cover the theme of this workshop?

  o Should we offer WP3 again in the future? At ISCA or MICRO? How can we improve the quality and the end utility?