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HiPINEB 2018

The 4th IEEE International Workshop on High-Performance Interconnection Networks in the Exascale and Big-Data Era

Viena, Austria, February 25, 2018

http://hipineb.i3a.info/hipineb2018/

To be held in conjunction with the HPCA Conference 2018

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ABSTRACT

By the year 2023, High-Performance Computing (HPC) Systems are expected to break the performance barrier of the Exaflop (10^18 FLOPS) while their power consumption is kept at current levels (or increases marginally), what is known as the Exascale challenge. In addition, more storage capacity and data-access speed is demanded to HPC clusters and datacenters to manage and store huge amounts of data produced by software applications, what is known as the Big-Data challenge. Indeed, both the Exascale and Big-Data challenges are driving the technological revolution of this decade, motivating big research and development efforts from industry and academia. In this context, the interconnection network plays an essential role in the architecture of HPC systems and datacenters, as the number of processing or storage nodes to be interconnected in these systems is very likely to grow significantly to meet the higher computing and storage demands. Besides, the capacity of the network links is expected to grow, as the roadmaps of several interconnect standards forecast. Therefore, the interconnection network should provide a high communication bandwidth and low latency, otherwise the network would become the bottleneck of the entire system. In that regard, many design aspects are considered when it comes to improving the interconnection network performance, such as topology, routing algorithm, power consumption, reliability and fault tolerance, congestion control, programming models, control software, etc.

The main goal of the fourth edition of HiPINEB is to gather and discuss in a full-day event the latest and most prominent efforts and advances, from both industry and academia, in the design and development of scalable high-performance interconnection networks, especially those oriented to meet the Exascale challenge and Big-data demands.

All researchers and professionals, from both industry and academia, working in the area of interconnection networks for scalable HPC systems and Datacenters are encouraged to submit an original paper to the workshop and to attend this event.

PROGRAM HIGHLIGHTS

* Keynote titled "The three L's in modern high-performance networking: Low latency, Low cost, Low processing load", will be given by Torsten Hoefler, ETH Zürich.

* Selected papers will be invited to submit and extended version to a Special Issue of Elsevier Journal of Parallel and Distributed Computing (JPDC).

* Panel session: "Industrial perspective of high-speed communication technology evolution", moderated by Dr. Young Cho, Research Assistant Professor of Computer Science in University of Southern California, Viterbi School of Engineering, and the USC Information Sciences Institute (ISI).

TOPICS OF INTEREST

The list of topics covered by this workshop includes, but is not limited to, the following:

* Interconnect architectures and network technologies for high-speed, low-latency interconnects.

* Scalable network topologies, suitable for interconnecting a huge number of nodes.

* Power saving policies in the interconnect devices and network infrastructure, both at software and hardware level.

* Good practices in the configuration of the network control software.

* Network communication protocols: MPI, RDMA, MapReduce, etc.

* APIs and support for programming models.

* Routing algorithms.

* Quality of Service (QoS).

* Reliability and Fault tolerance.

* Load balancing and traffic scheduling.

* Network Virtualization.

* Congestion Management.

* Applications and Traffic characterization.

* Modeling and simulation tools.

* Performance Evaluation.

* Interfacing accelerators through the interconnect (GPUs, Xeon Phi, etc).

* Network infrastructure in distributed storage, distributed databases and Big-Data.

Furthermore, short papers in the above topics will be also taken into consideration, as long as they are based on emerging ideas, work-in-progress and early, high-impact achievements.

Note, however, that papers focused on topics that are too far from the design, development and configuration of high-performance interconnects for HPC systems and Datacenters (e.g., mobile networks, intrusion detection, peer-to-peer networks or grid/cloud computing) will be automatically considered as out of scope and rejected without review.

PAPER SUBMISSIONS

Regular and short papers must be in PDF format and should include title, authors and affiliations as well as the e-mail address of the contact author. Submitted regular manuscripts may not exceed 8 single-spaced double-column pages using 10-point size font on 8.5x11 inch pages, including figures, tables, and references. Short papers may not exceed 4 single-spaced double-column pages using 10-point size font on 8.5x11 inch pages. At least one author of the paper must be registered for the conference workshop. The conference style is based on IEEE (available at:
http://www.ieee.org/conferences_events/conferences/publishing/templates.html).

HiPINEB manuscript submissions are managed by easyChair. To submit a paper, go to https://easychair.org/conferences/?conf=hipineb2018 and follow the instructions.

REVIEW PROCESS

Authors are entitled to submit original papers of high technical quality, according to the list of topics described above. Papers will be reviewed based on originality, novelty, technical strength, presentation quality, correctness and relevance to the conference scope.

WORKSHOP PROCEEDINGS

Papers will be published in the HiPINEB proceedings, edited by the IEEE CPS which will be submitted for indexing and inclusion in IEEE Xplore and CSDL.

SPECIAL ISSUE

Best papers among those selected for HiPINEB 2018 will be invited to submit and extended version to the Journal of Parallel and Distributed Computing (JPDC), Elsevier, 2016 Impact Factor: 1.930. Further details provided soon in http://hipineb.i3a.info/hipineb2018/special-issue

IMPORTANT DATES

Submission Opens: October 20, 2017

Paper submission due: January 8, 2018

Notification of acceptance: January 31, 2018

Early Registration due: TBA

Camera-ready papers due: February 5, 2018

Workshop date: February 24,2018

All deadlines are set at 11:59 p.m. anywhere on Earth

(cf. http://wirelessman.org/aoe.html).

WORKSHOP ORGANIZATION

Organizers:

* Pedro Javier Garcia, University of Castilla-La Mancha, Spain

* Jesus Escudero-Sahuquillo, University of Castilla-La Mancha, Spain

Steering Committee:

* Jose Duato, Technical University of Valencia, Spain
* Francisco Jose Quiles, University of Castilla-La Mancha, Spain
* Torsten Hoefler, ETH Zurich, Switzerland
* Timothy M. Pinkston, University of Southern California, USA
* Eitan Zahavi, Mellanox, Israel

Program Committee:

* Francisco J. Alfaro, University of Castilla-La Mancha, Spain
* Jose Cano-Reyes, University of Edinburgh, United Kingdom
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* John Kim, KAIST, South Korea
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* Matthieu Perotin, ATOS/BULL, France

* Mikel Eukeni Pozo Astigarraga, CERN, Switzerland

* Samuel Rodrigo, Skala Norge AS, Norway

* Sebastien Rumley, Columbia University, USA

* Jose Luis Sanchez, University of Castilla-La Mancha, Spain

* Jörn Schumacher, CERN, Switzerland

* Alex Shpiner, Mellanox Technologies, Israel

* Evangelos Tasoulas, Simula Research Laboratory, Norway

* Luis Tomas Bolivar, Red Hat, Spain

* Enrique Vallejo, University of Cantabria, Spain

* Peng Zhang, Stony Brook University, USA

* TBC...

ADDITIONAL INFORMATION

For more information on HiPINEB 2018 check the website at:
http://hipineb.i3a.info/hipineb2018

or, if you have any question, please contact the workshop organizers at hipineb@dsi.uclm.es